AN-CM2309

POWERMASTER SEMICONDUCTOR

Masters of Power Solution

650V eSiC M1 MOSFET Series

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1. Introduction

The digital transformation that many companies underwent during the pandemic has continued to impact the world. Recently, the rapid growth of artificial intelligence (AI) is expected to drive a strong data center demand. This will spur innovations in data center design and technology to deliver the capacity that meets the increased power density requirements of high-performance computing. Therefore, data centers, cloud servers, and 5G telecom power supplies are still experiencing rapid growth. Future requirements for power supplies will require a simultaneous increase in power density along with increased operating efficiency. As an example, 80 Plus Titanium will be a mandatory requirement for single output power supply units (PSU) by 2023 and all PSUs by 2026. (System efficiency > 90% at 10% load, System efficiency must achieve > 96% at 50% load) as shown in Fig 1. In general, the light and medium load efficiency is becoming more critical for 80 PLUS titanium. Si Super-junction MOSFETs have been widely used for the 400~900V range in power conversion applications such as the power factor correction and primary switch for DC-DC converters. However, Si Super-junction MOSFETs already have trouble meeting the Platinum specifications. In response to these requirements, engineers are exploring alternative devices to design innovative and high-performance PSU's that further shrink footprints while challenging both thermal and electrical characteristics of power devices.

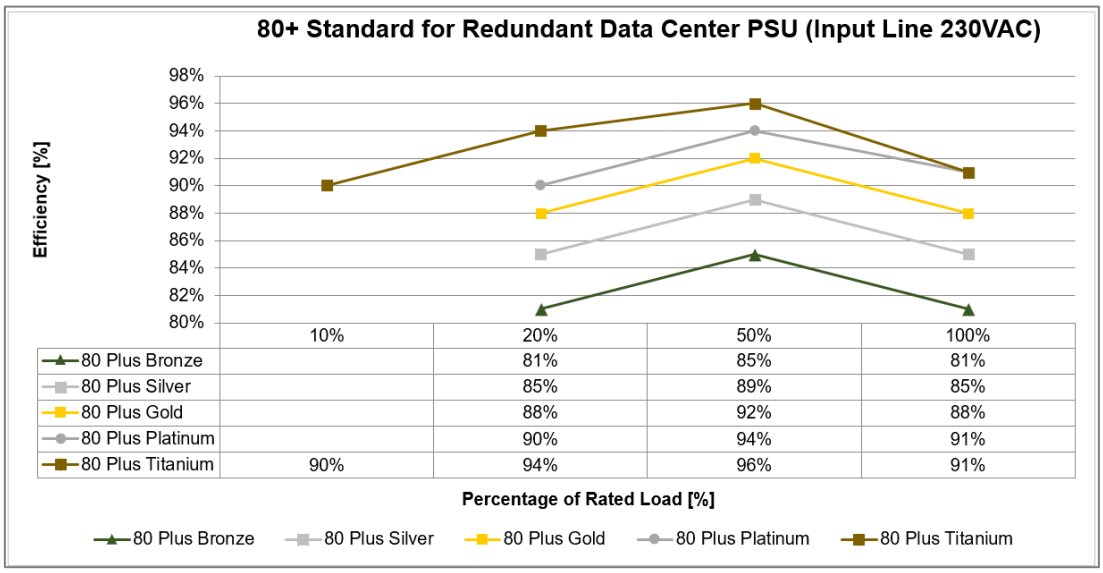


Figure 1. 80 Plus standard for redundant / data center PSU (Input line 230VAC)

Therefore, the 650V WBG power devices are quickly penetrating the server, telecom, and data center AC/DC power supply units (PSUs) due to their combined low $R_{DS(ON)}$, low capacitances, and very low diode recovery charge, Q_{RR} compared to silicon devices. These are the main features that are required for enabling increased power density and system efficiency demands of the next generation PSUs. Requirements for increased power density and efficiency drive the need for more advanced circuit topologies that generally require the power switch to operate at higher switching frequencies (F_{sw}). This places a strong demand on the need for very low switching losses, which are gauged by some of the device figures-of merit (FOM's: $R_{DS(ON)}$ x Q_G, $R_{DS(ON)}$ x Q_{OSS}, $R_{DS(ON)}$ x Q_{RR}). Many PSUs still use Si Super-junction MOSFETs, but SiC MOSFETs are being adopted very quickly and are replacing Super-junction MOSFETs in some key sockets for advanced topologies such as Totem Pole PFC and high frequency LLC resonant converters. The 650V~750V SiC MOSFET is also widely used for on-board chargers (OBCs). The purpose of this application note is to highlight the key characteristics of Power Master Semiconductor's new 650V eSiC MOSFET M1 compared to competitor's 650V trench and planar SiC MOSFETs.

2. Target Applications of 650V eSiC M1 MOSFET

SiC MOSFETs exhibit higher breakdown voltage, higher operating temperature, higher thermal conductivity, and lower conduction and switching losses compared to silicon MOSFETs. The 650V SiC MOSFETs offer significant system advantages such as smaller, lighter, higher efficiency, and less cooling effort thanks to their much lower power losses in various power conversion applications. Therefore, 650V SiC MOSFETs are gaining popularity especially for data center, cloud servers, 5G telecom power supplies, motor control, energy storage system (ESS), Solar and electric vehicle charging system applications that required high frequency operation and higher efficiency as shown in Fig 2. The on-board charger (OBC) is an essential block into the xEV to recharge high voltage battery from the AC grid. The OBC power rating is increasing from 6.6kW to 11~22kW. Bi-directional operation is the key trend for the next on-board charger (OBC) application for V2L (Vehicle to Load), V2G (Vehicle to Grid), V2V (Vehicle to Vehicle), and V2H (Vehicle to Home appliances). Therefore, topology is moving to Totem-pole PFC + CLLC or DAP resonant converter from Interleaved CCM PFC or Dual boost bridgeless PFC + LLC resonant converters. The 650V SiC MOSFET is suitable for 400V battery OBC systems. Power Master Semiconductor's new 650V eSiC MOSFET M1 provides the excellent switching performance and higher ruggedness, while providing ultra-low $R_{DS(ON)}$.

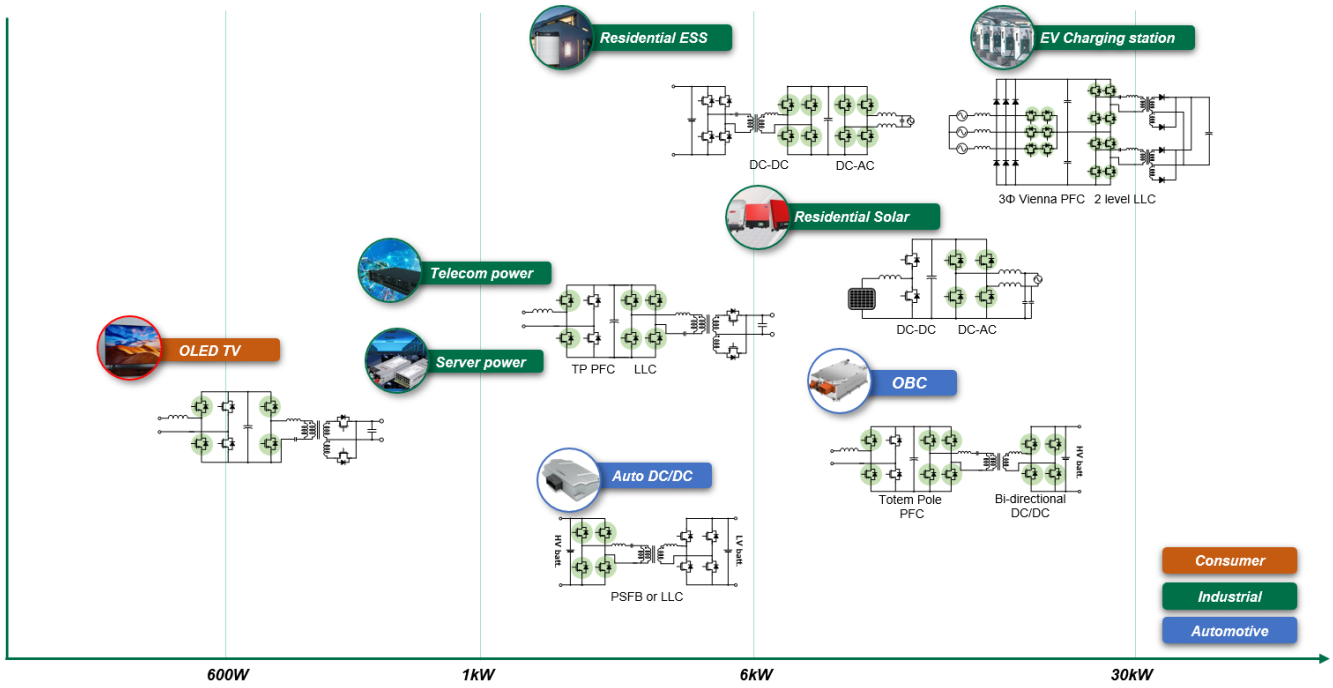
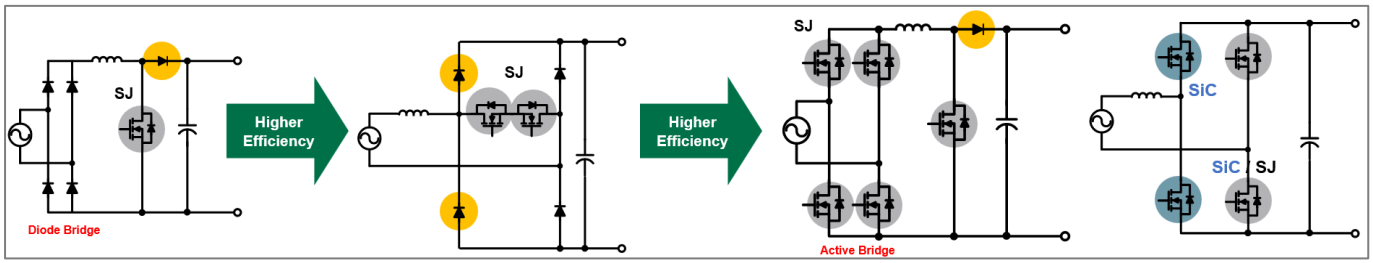


Figure 2. Target Applications of 650V SiC MOSFET.

2.1. Power Factor Correction (PFC) Topology Trend

Grid-interfaced AC/DC power supplies typically consist of a power factor correction (PFC) stage and a DC-DC stage that is usually an LLC converter. The requirement for higher system efficiency combined with higher power density drives the need for both better semiconductor devices as well as better topologies. The high-end (or high efficiency) PFC stage is transitioning away from the standard diode bridge combined with a classic boost stage to more efficient semi-bridgeless or active bridge stages as shown in Fig. 3. The active bridge PFC can simply replace the 4x diode in the bridge with low $R_{DS(ON)}$ MOSFETs. The BOM cost and complexity rises, but the efficiency increases. The Totem Pole PFC combines the PFC stage and diode bridge into one stage. This topology is rapidly becoming the topology of choice for high-end PFCs.



(a) Classic Boost PFC (b) H-PFC(Semi-Bridgeless) (c) Active-Bridge SR + Boost PFC (d) Totem-pole PFC

Figure 3. Power Factor Correction (PFC) Evolution (left to right). Move towards Bridgeless PFC (active bridge SR or Totem-pole)

The purpose of this application note is to highlight the key characteristics of Power Master Semiconductor's new 650V *e*SiC MOSFET M1 compared to trench and planar competitor's 650V SiC MOSFETs.

2.2. Key parameters for Totem-pole PFC

The operation of CCM Totem Pole PFC can be simply divided into four phases during the positive and negative cycles of AC input voltage as shown in Fig. 4.

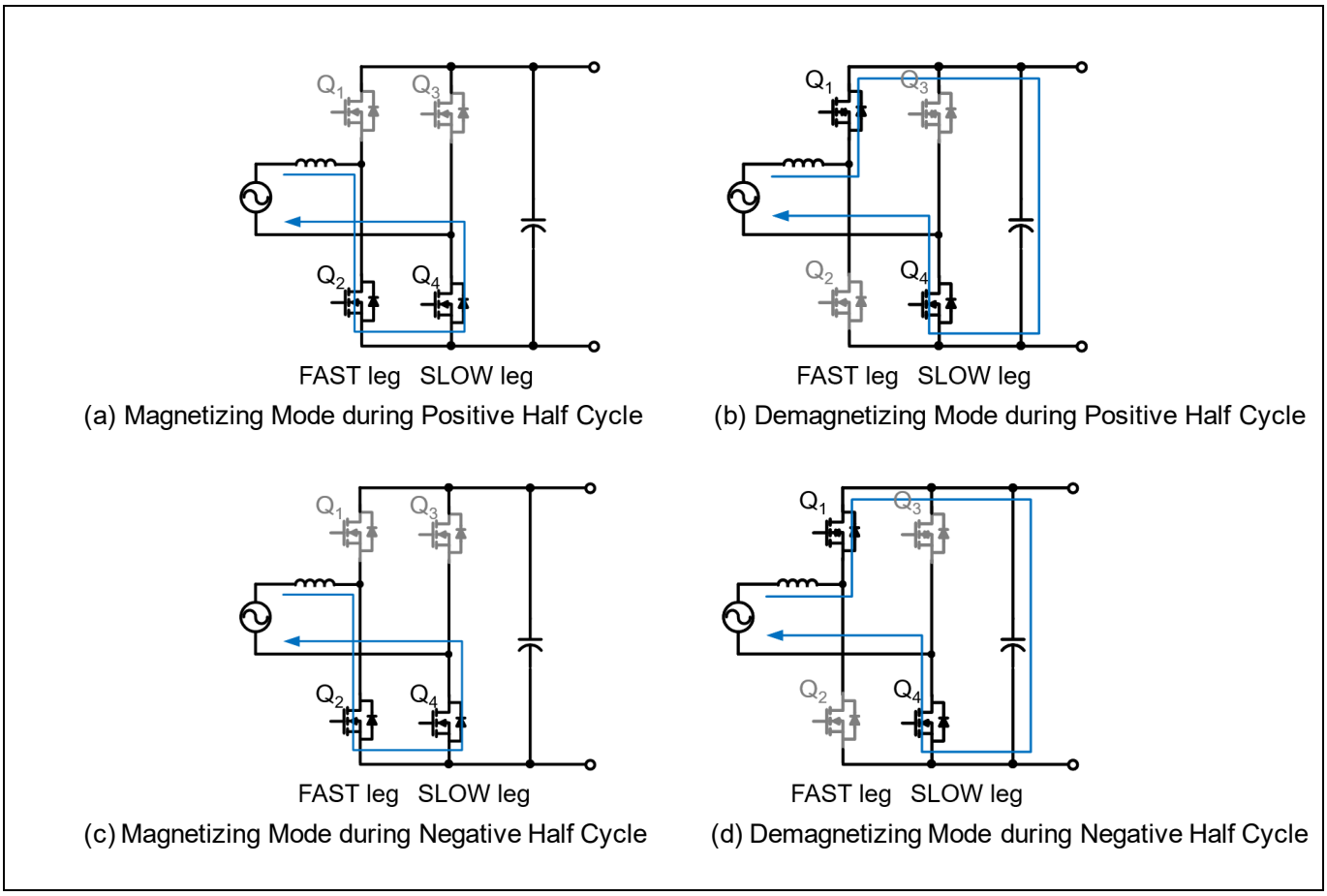


Figure 4. Totem-Pole PFC Operation during Positive and Negative Half Cycle

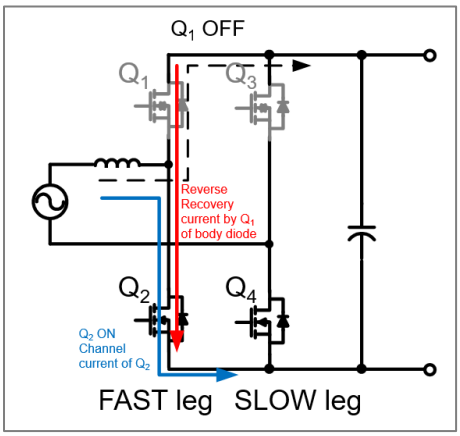


Figure 5. Hard commutation on body diode of FAST leg MOSFET in a Totem-Pole PFC

The Totem Pole PFC consists of four MOSFETs, two MOSFETs (Q_1 and Q_2) reside in the "FAST" leg of the bridge and two MOSFETs (Q_3 and Q_4) reside in the "SLOW leg". The requirements between the two legs are much different. During positive AC cycle, Q_4 of "SLOW" leg is continuously conducting. "FAST" leg switches (Q_1 and Q_2) with the PFC inductor create a synchronous mode boost converter. The boost switch, Q_2 is turned on to magnetize the PFC inductor during magnetizing mode as shown in Fig.4 (a). After Q_2 turns off, the body diode of Q_1 is conducts before Q_1 turns on as a synchronous switch during demagnetizing mode as shown in Fig 4 (b). When Q_1 is turns off, inductor current flows through body diode of Q_1. Simultaneously, Q_2 is turns on while Q_1 is turns off, body diode reverse recovery and discharge current of Q1 flows through the MOSFET Q_2 due to hard commutation of Q_1 body as shown in Fig. 5. During the negative half cycle, the operation is similar except that the role of "FAST" leg switches is swapped and Q_3 of "SLOW" leg is continuously conducting.as shown in Fig. 4 (c) and (d). the hard commutation occurs in every switching cycle on one of "FAST" leg switches. Therefore, turn-on switching loss of "FAST" leg switches is highly depends on the body diode Q_{RR} and Q_{OSS} of "FAST" leg switches. Therefore, the FAST leg switches are mostly dominated by SiC MOSFET and GaN devices today. The "SLOW" leg switches, which are mainly dominated by Super-junction MOSFETs require low $R_{DS(ON)}$ and robustness to surge current. Key parameters of "FAST" leg switches for Totem-pole PFC are shown in below.

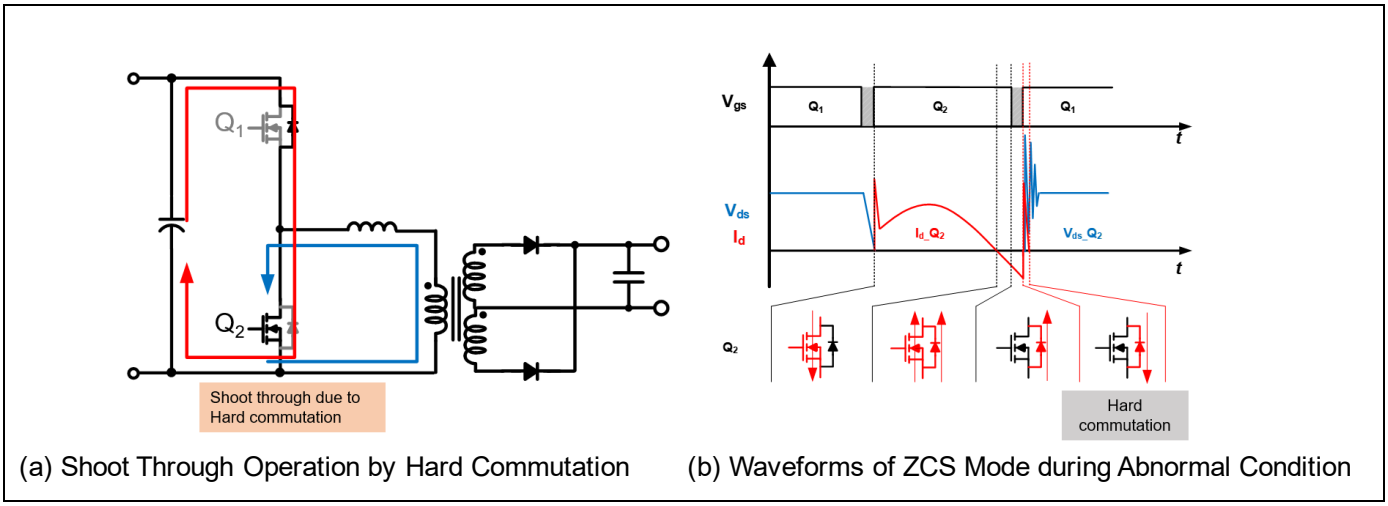
Key parameters of FAST leg switch for Totem-pole PFC

- Low FOM : $R_{DS(ON)}$ * Q_G for higher heavy load efficiency.
- Low E_{OSS} for higher light load efficiency.
- Low Q_{RR} of body diode for lower turn-on loss.
- Low V_{SD} of body diode.
- Low switching losses.
- Reasonable V_{DS} overshoot and gate oscillation.

2.3. Key parameters for LLC Resonant Converter

The LLC converter is widely used in DC/DC stages for various AC-DC applications, including server/telecom powers, on board chargers (OBC), EV charging station (EVC), etc. The LLC resonant converter requires a MOSFET with robust body diode characteristic because there is hard commutation of body diode during start-up or output short condition as shown in Fig. 6. Body diode reverse recovery is switching process where the body diode from on state to reverse blocking state. When reverse voltage is applied across the body diode, the stored charge should be removed to go back to blocking state. The removal of the stored charge occurs via two phenomena: the flow of a large reverse current and recombination. This reverse-recovery current flows through the body diode of MOSFET

because the channel is already closed. This reverse recovery current and displacement current can trigger the parasitic BJT. Once the parasitic BJT turns on, a hot spot is formed, and more current crowding occurs. More current flows through the parasitic BJT due to its negative temperature coefficient. Finally, the MOSFET can be failed.



(a) Shoot Through Operation by Hard Commutation (b) Waveforms of ZCS Mode during Abnormal Condition

Figure 6. Shoot Through Operation by Hard Commutation of Body Diode during Abnormal Operation in LLC Resonant Converter

In LLC resonant applications, Q_{OSS} is directly related to the charge which has to be provided and also the time needed to rise or fall the reverse voltage. The dead time between the high side and low side MOSFETs in the same leg must be long enough to allow the voltage transition. As shown in Fig. 7, MOSFETs that has smaller Q_{OSS} provide wider ZVS window at same dead time than that has larger Q_{OSS}. Therefore, circuit designers are able to increase switching frequency and losses for high power density by using low Q_{OSS} devices.

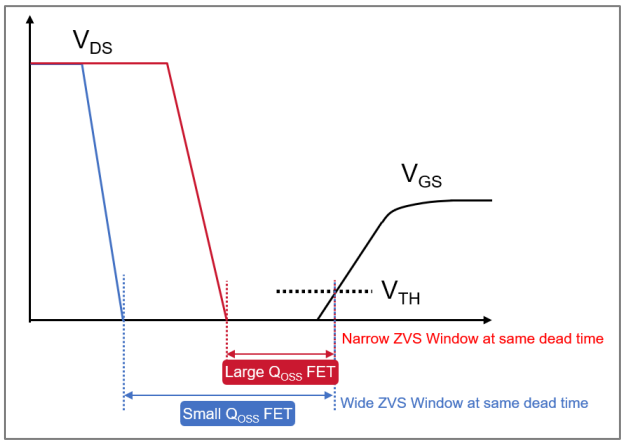


Figure 7. Dead time margin by Q_{OSS}

Super-junction MOSFETs have been utilized in LLC resonant converters due to its low $R_{DS(ON)}$ and E_{OSS} but its large Q_{OSS}, Q_{RR} and the snappy reverse recovery performance of the super-junction MOSFET's body diode is not attractive for high power density and reliability system [1]. Extremely low Q_{RR}, Q_{OSS} and Q_G of SiC MOSFET enable improved system reliability during abnormal operating condition and high-power density by higher frequency operation. Additionally, SiC MOSFET's lower E_{Dyn}, which is proportional to the switching frequency can improve light load efficiency in LLC resonant topologies. Key parameters of primary switches for LLC resonant converters are shown below.

Key parameters of primary side switch for LLC resonant converter

- Conduction losses, which are dominated by $R_{DS(ON)}$ and its temperature coefficient.
- Low dynamic C_{OSS} (E_{DYN}) Loss for higher efficiency in light load.
- Soft reverse recovery and ruggedness of body diode for better system reliability under abnormal condition.
- Small Q_{OSS} for short dead-time to minimize duty loss.
- Low Q_G for fully turn-on under light load and standby condition.

3. 650V eSiC MOSFET M1 Technology

Two typical structures (planar and trench) of SiC MOSFET are available today, SiC MOSFET structures depend on the performance of the device, strategy, the target applications [2]~[4]. The planar structure is easier to fabricate but has the disadvantage of having a higher R_{SP} (Resistance per unit area) compared to the same rating trench one. This is due to the channel current flowing perpendicularly to the vertical direction and the existence of the inner JFET region. Trench structure is good to reduce both $R_{DS(ON)}$ and switching performance because, the main reason is that the electron mobility of the channel formed in the trench sidewall is greater than that of the surface part. but disadvantage of trench is that need complex SiC trench etching process and lower ruggedness compared to planar structure. 650V eSiC M1 technology is Power Master Semiconductor's first generation of SiC MOSFET.

3.1. Performance benchmark of 650V SiC MOSFETs

Table 1 shows the key parameter comparison of 650V SiC MOSFETs. Advantages of 650V eSiC MOSFET M1 (PCZ65N45M1) are the reduced switching losses, dynamic C_{OSS} losses (E_{Dyn}) and robust avalanche capability for both high system efficiency and reliability.

Table 1. Key Parameter Comparison of Power Master Semiconductor's 650V/45mΩ eSiC MOSFET M1 (PCZ65N45M1) and Competitors

Specification	PCZ65N45M1	Comp. A (Planar)	Comp. B (Planar)	Comp. C (Trench)
BV_{DSS} [V]	650	650	650	650
I_D [A]	42	49	47	39
V_{GS_op} [V]	-5 / +18	-4 / +15	-5 / +18	0 / +18
V_{GS_max} [V]	-10 / +22	-8 / +19	-10 / +22	-5 / +23(pulse)
$R_{DS(on)}$ [mΩ] (typ)	45	45	44	45
V_{TH} [V]	1.8 / 2.8 / 4.5	1.8 / 2.6 / 3.6	1.8 / 2.8 / 4.3	3.5 / 4.5 / 5.7
E_{DYN} [uJ]	1.2	1.4	2.0	1.5
Q_G [nC]	55	63	74	33
E_{ON} [μJ] @ I_D=20A, R_G=2.7Ω	33	48	78	43
E_{OFF} [μJ] @ I_D=20A, R_G=2.7Ω	14	17	25	18
I_{AS} @ L=1mH, R_G=25Ω	34	30	15	21

3.1.1. Dynamic C_{OSS}, E_{Dyn}

Recently, power loss by hysteresis C_{OSS} is analyzed in many papers [5]~[7]. Unexpected power losses associated especially for SJ MOSFETs in ZVS topologies, are generated due to the hysteretic phenomenon of the output capacitance, C_{OSS}. These power losses related to C_{OSS} hysteresis are more critical in soft switching topologies such as LLC when operating under high frequency conditions, especially in medium and light loads. Consequently, a certain amount of energy is generated. Dynamic C_{OSS} loss (E_{Dyn}) can be defined as the difference between charging energy and discharge energy except some lost energy during discharging process. This energy losses can be observed by hysteresis loop area large signal C_{OSS} during charge-discharge cycle as shown in Fig. 8. The dynamic C_{OSS} losses (E_{Dyn}) are affected by device structure especially termination area, die size, switching dV_{DS}/dt in SiC MOSFETs. [6]

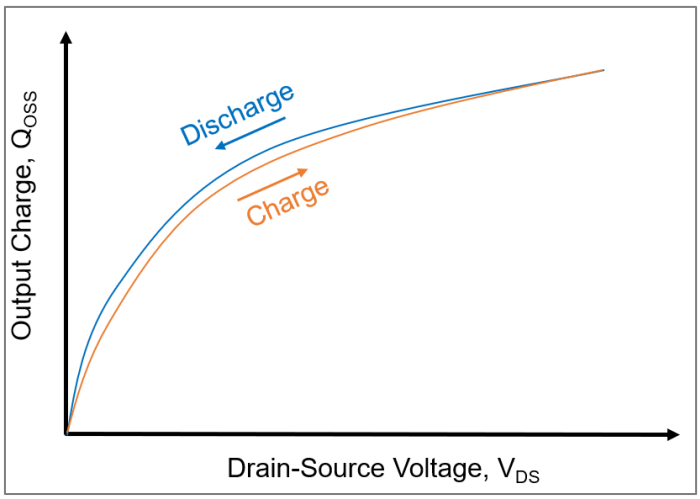


Figure 8. Hysteresis Charging and Discharging of C_{OSS}

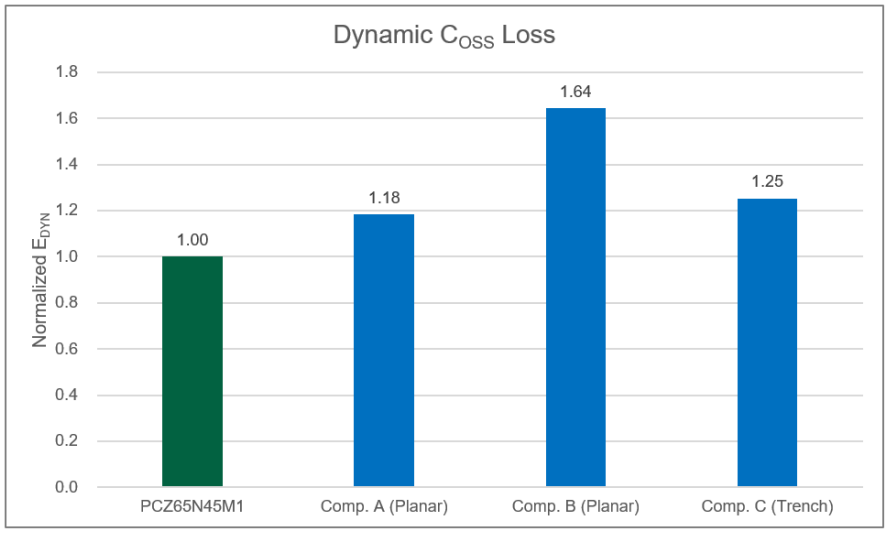


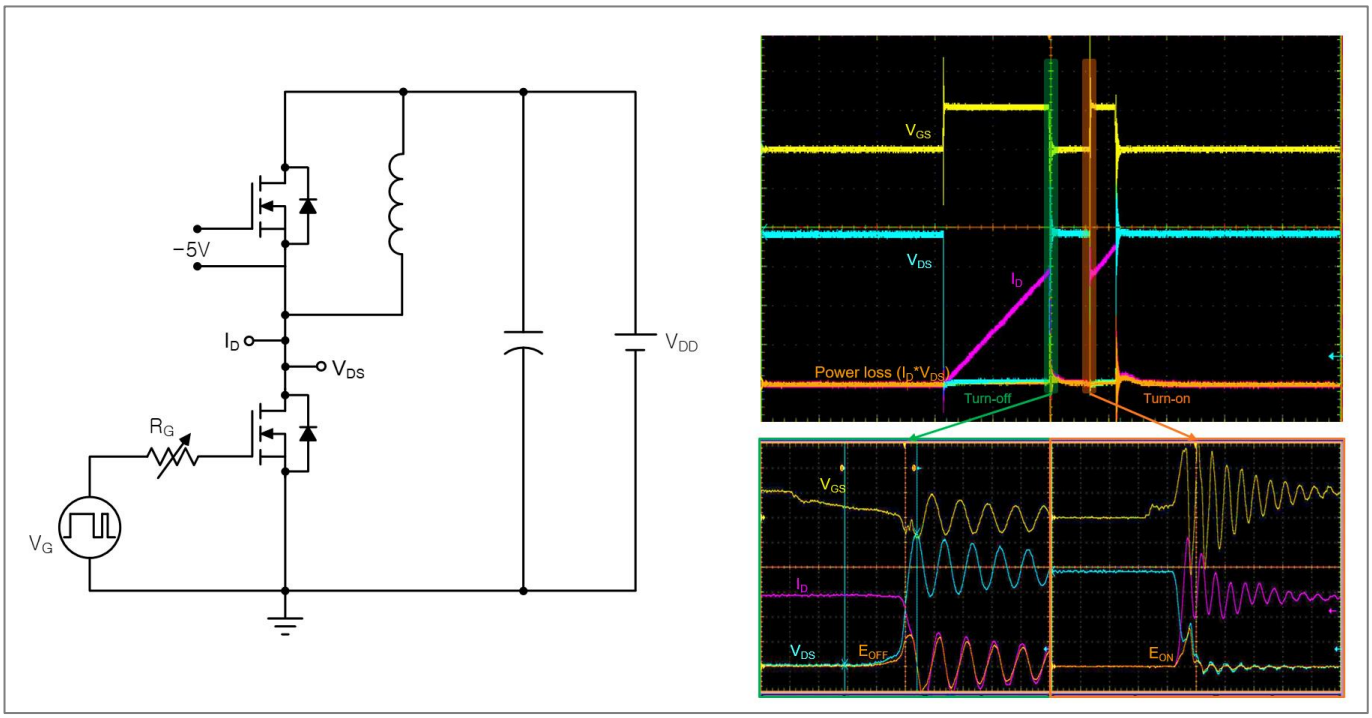
Figure 9. Normalized Dynamic C_{OSS} loss of 650V *e*SiC MOSFET M1 (PCZ65N45M1) vs. Competitors

Fig. 9 shows a normalized dynamic C_{OSS} loss of the 650V *e*SiC MOSFET M1 (PCN65N45M1), and its competitor under same condition, V_{DS}=0~400 V. The dynamic C_{OSS} loss of 650V *e*SiC MOSFET M1 (PCN65N45M1) is 15~39% less than that of both planar and trench SiC competitors.

3.1.1.1. Switching Characteristics

The double pulse test, which involves applying two pulses to the gate of MOSFET, resulting in both turn-off and turn-on events, is conducted with an inductive load, a power supply and pulse generator. In real application, the main inductive load is clamped, therefore, double pulse test is also called inductive switching test. Double-pulse testing is a popular method for investigating dynamic switching performance of power devices as shown in Fig. 10. Double pulse test is helpful to not only estimate switching losses (E_{on} and E_{off}), and noise (peak drain-source voltage, gate ringing and turn-off dv/dt) but also understand the parasitic behaviors of the devices. As the circuit isn't operated continuously during this test, the self-heating of the switches and inductor is considered negligible. Therefore, clamped inductive switching test, which is a good representation for a boost converter, is very commonly used as a benchmark for evaluating the performance of the switching devices.

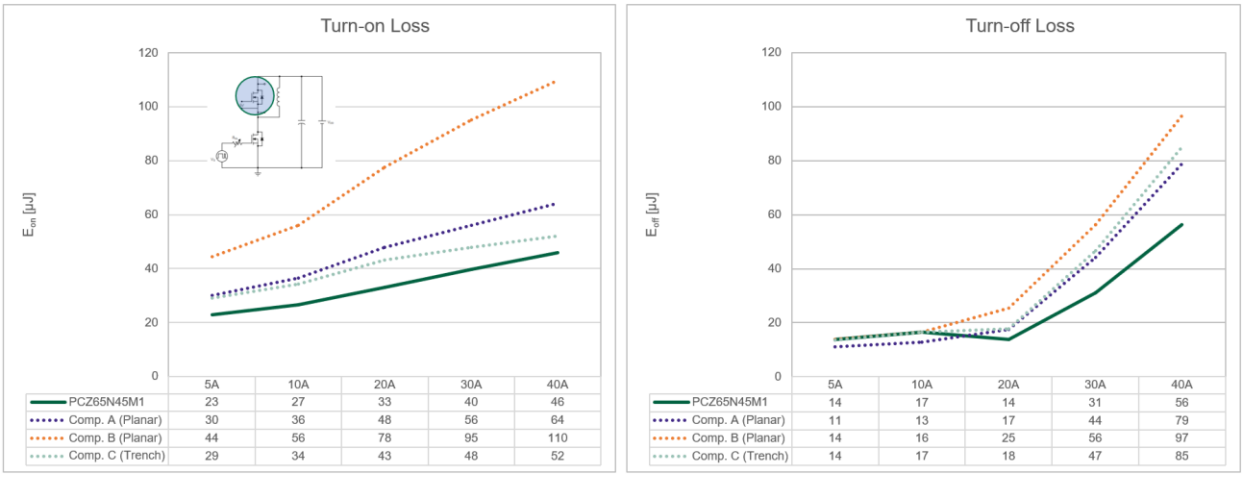
The double pulse test involves applying two pulses to the gate of a MOSFET, resulting in both turn-off and turn-on events at the desire current level. This test is conducted with an inductive load, a power supply, and a pulse generator. In real applications, the main inductive load is clamped, hence the double pulse test is also referred to as an inductive switching test. Double-pulse testing is a popular method for investigating the dynamic switching performance of power devices, as shown in Fig. 10. It is helpful not only for estimating switching losses (Eon and Eoff) and switching noise (peak drain-source voltage, gate ringing, and turn-off dv/dt) but also for understanding the parasitic behaviors of the devices. Since the circuit is not operated continuously during this test, the self-heating of the switches and inductor is considered negligible. Therefore, the double pulse test, which is a good representation for a boost converter, is commonly used as a benchmark for evaluating the performance of switching devices.



(a) Double Pulse Test Circuit (b) Voltage and Current Waveforms during Double Pulse Test

Figure 10. Switching Performance Measurements with Double Pulse Test Board

Fig. 11 shows the measured switching losses (E_{on} and E_{off}) comparisons of 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) and competitors (trench and planar). The measurement is performed using the body diode of same DUT as a freewheeling diode in the high side device, with V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, under various I_D conditions. Turn-on loss (E_{on}) is 17% and 58% less and turn-off loss (E_{off}) is 29% and 45% less for 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) compared to that of competitor C (trench) and competitor B (planar) under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=30A, FWD=Same DUT.

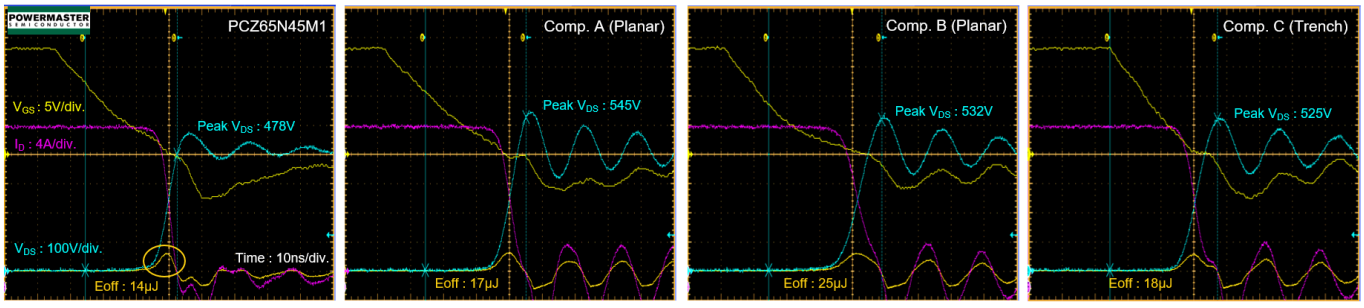


	5A	10A	20A	30A	40A
PCZ65N45M1	23	27	33	40	46
Comp. A (Planar)	30	36	48	56	64
Comp. B (Planar)	44	56	78	95	110
Comp. C (Trench)	29	34	43	48	52

	5A	10A	20A	30A	40A
PCZ65N45M1	14	17	14	31	56
Comp. A (Planar)	11	13	17	44	79
Comp. B (Planar)	14	16	25	56	97
Comp. C (Trench)	14	17	18	47	85

Figure 11. Comparison of Switching Losses - 650V/45mΩ *e*SiC MOSFET M1(PCZ65N45M1) vs. competitors under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, Free-wheeling Diode: Same DUT

Fig. 12. shows the SiC MOSFET turn-off waveforms under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=20A with FWD=the same DUT. As shown in Fig. 12, 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) significantly reduces both turn-off loss and drain-source voltage spikes, which are typically in trade-off by its optimized design. Turn-off loss (E_{off}) is 22% less and peak drain-source voltage is 47V lower for 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) even compared to those of competitor C(trench). Furthermore, the voltage and current ringing of 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) are significantly reduced compared to competitors.

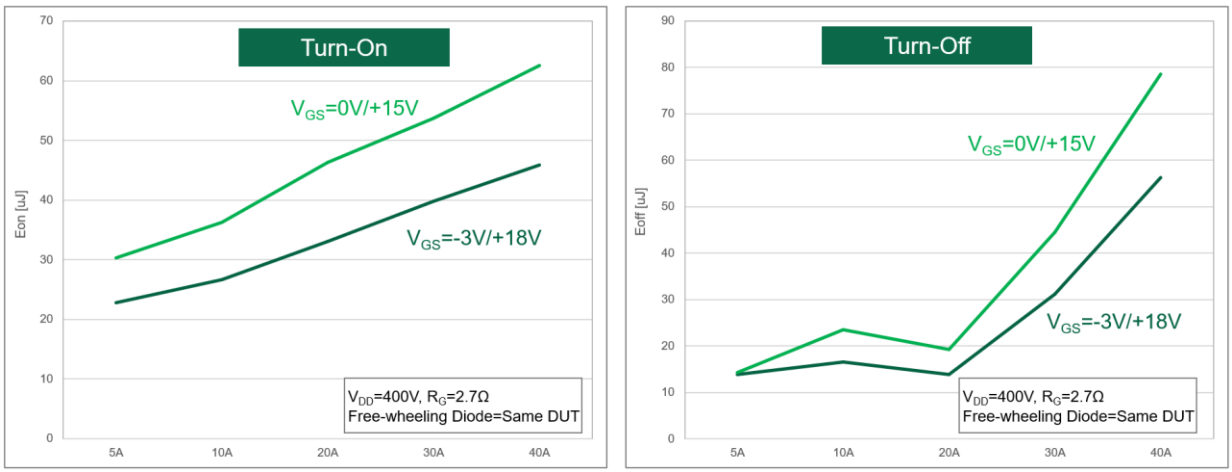


(a) PCZ65N45M1 (b) Comp. A (Planar) (c) Comp. B (Planar) (d) Comp. C (Trench)

Figure 12. Comparison of Switching Waveforms at Turn-Off Transient - 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) vs. Planar and Trench Competitors under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=20A, Freewheeling Diode: Same DUT

3.1.2. Switching Behavior vs. Gate Driving Voltage (V_{GS})

Unlike Super-junction MOSFETs, which typically use 0~10V, SiC MOSFETs require higher gate driving voltage (V_{GS}) swing typically, -5~+18V due to challenges such as lower channel mobility. Fig. 13. shows different switching loss by gate driving voltage of 650V/45mΩ eSiC MOSFET M1. As positive gate voltage increases, turn-on switching loss decreases, while turn-off loss remains similar as shown in Fig. 13 (a). However, higher gate voltage imposes more stress on gate oxide, potentially resulting in $V_{GS(TH)}$ drift. As negative gate voltage increases, turn-off switching loss decreases, while turn-on loss remains similar as shown in Fig. 13 (b). As a results, E_{on} at $V_{GS(on)}$=18V is reduced 26% compared with $V_{GS(on)}$=15V and E_{off} at $V_{GS(off)}$=-3V is reduced 30% compared with $V_{GS(off)}$ =0V at I_D=30A.



(a) Turn-on Loss (E_{on}) vs V_{GS} (b) Turn-off Loss (E_{off}) vs V_{GS}

Figure 13. Switching Losses vs. V_{GS} of 650V/45mΩ eSiC MOSFET M1(PCZ65N45M1) under V_{DD}=400V, V_{GS}=-3V/+18V and 0V/15V, R_G=2.7Ω, Free-wheeling Diode=Same DUT

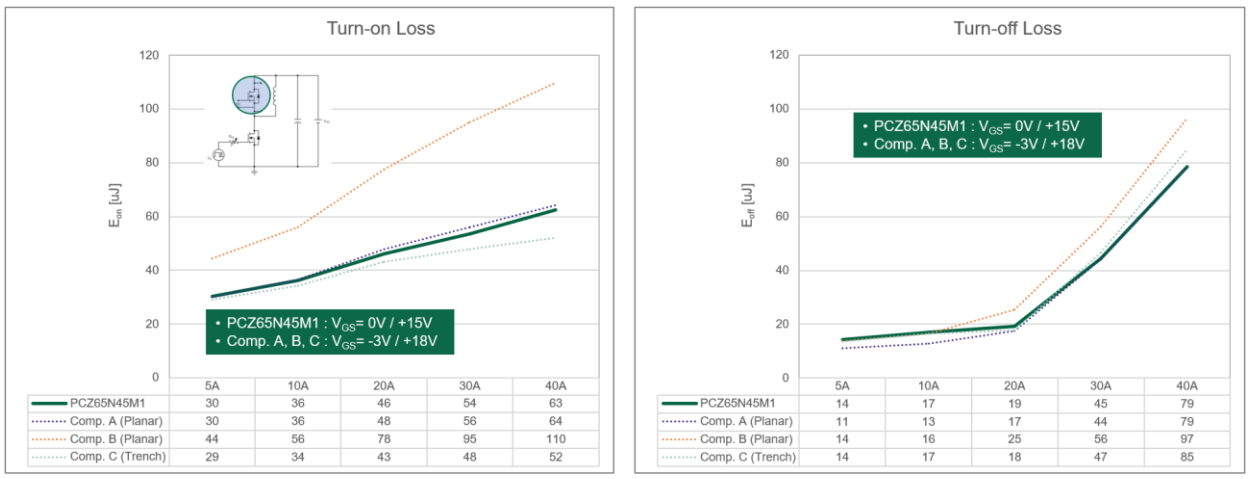
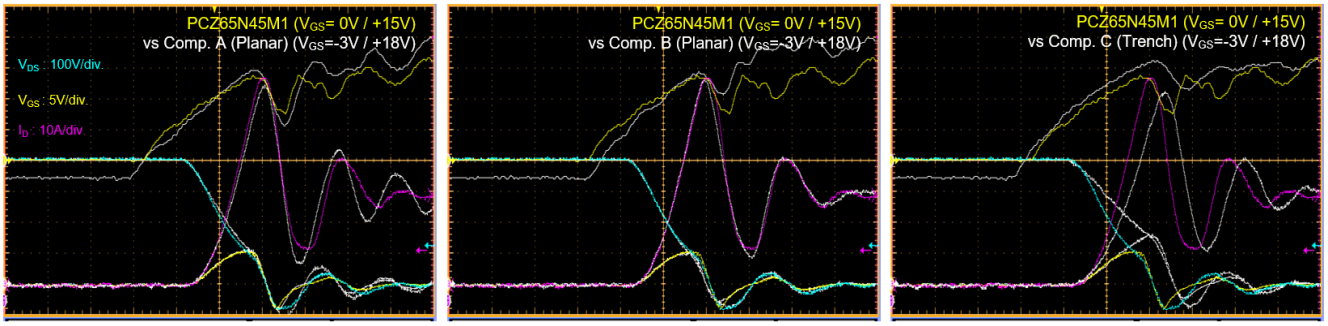
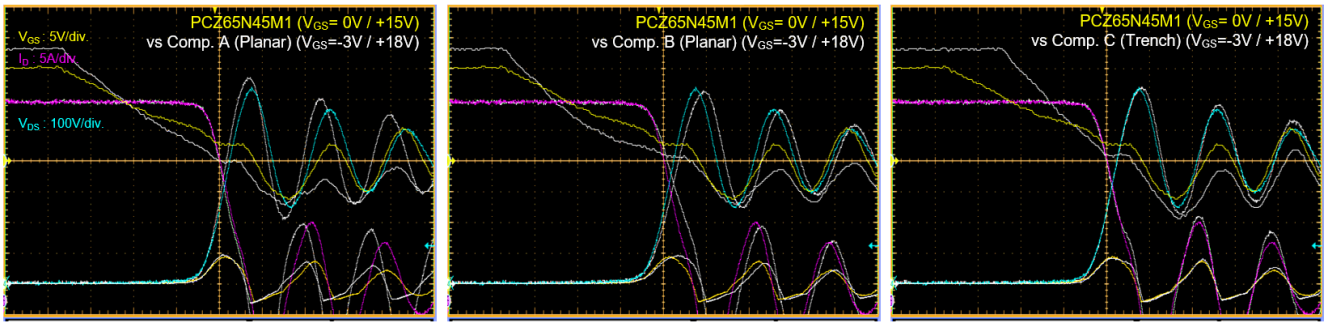


Figure 14. Comparison of Switching Losses vs V_{GS} - 650V/45mΩ eSiC MOSFET M1 (PCZ65N45M1) (V_{GS}=0V/+15V) vs. competitors (V_{GS}=-3V/+18V) under V_{DD}=400V, R_G=2.7Ω, Free-wheeling Diode: Same DUT

Fig. 14 shows the measured switching losses (E_{on} and E_{off}) for different V_{GS} of 650V/45mΩ eSiC MOSFET M1 (PCN65N45M1) and competitors (trench and planar). As shown in Fig. 14, the 650V/45mΩ eSiC MOSFET M1 (PCN65N45M1) shows similar or lower E_{on} and E_{off} with V_{GS}=0/+15V compared to that of competitors with V_{GS}=-3V/+18V under same conditions except gate driving voltage, V_{GS}.



(a) Turn-on Transient



(b) Turn-off Transient

Figure 15. Comparison of Switching Waveforms with Different V_{GS} of 650V/45mΩ eSiC MOSFET M1, PCN65N45M1 with V_{GS}=0V/+15V and competitors with V_{GS}=-3V/+18V under V_{DD}=400V, I_D=30A, R_G=2.7Ω, Free-wheeling Diode: Same DUT

As shown in Fig. 15, 650V/45mΩ eSiC MOSFET M1 (PCN65N45M1) shows similar switching waveforms with V_{GS}=0/+15V compared to competitors with V_{GS}=-3V/+18V under V_{DD}=400V, I_D=30A, R_G=2.7Ω, and free-wheeling Diode=the same DUT. Power Master recommends a $V_{GS(on)}$ of +18V as it can minimize both $R_{DS(on)}$ and turn-on switching loss. 650V eSiC MOSFET M1 can also be driven at lower gate driving voltages (15V) while maintaining similar turn-off loss compared to those of competitor's operation at $V_{GS(on)}$=18V. However $V_{GS(on)}$=15V operating will negatively affect to the $R_{DS(on)}$.

3.1.3. Avalanche Capability (E_{AS}: Single Pulsed Avalanche Energy & I_{AS}: Avalanche Current)

E_{AS} and I_{AS} represent the maximum energy level and maximum current level for a single pulse in avalanche breakdown mode, which is unclamped inductive switching condition. These values are ruggedness parameters of a MOSFET during the avalanche operation. The test circuit and waveform are shown in the Fig. 16. The current increases gradually and charges inductor energy by increasing pulse width during MOSFET turns-on. When MOSFET is turned off, the charged inductor energy causes the drain voltage to rise to MOSFET breakdown voltage, after which the inductor's charged energy decreases linearly.

The single pulsed energy is calculated with Equation 1)

Equation 1)

$$E_{AS} = \frac{1}{2} \times L \times {I_{AS}}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

L is inductor value, I_{AS} is single pulse avalanche current, BV_{DSS} is the breakdown voltage between drain to source, and V_{DD} is an applying DC voltage.

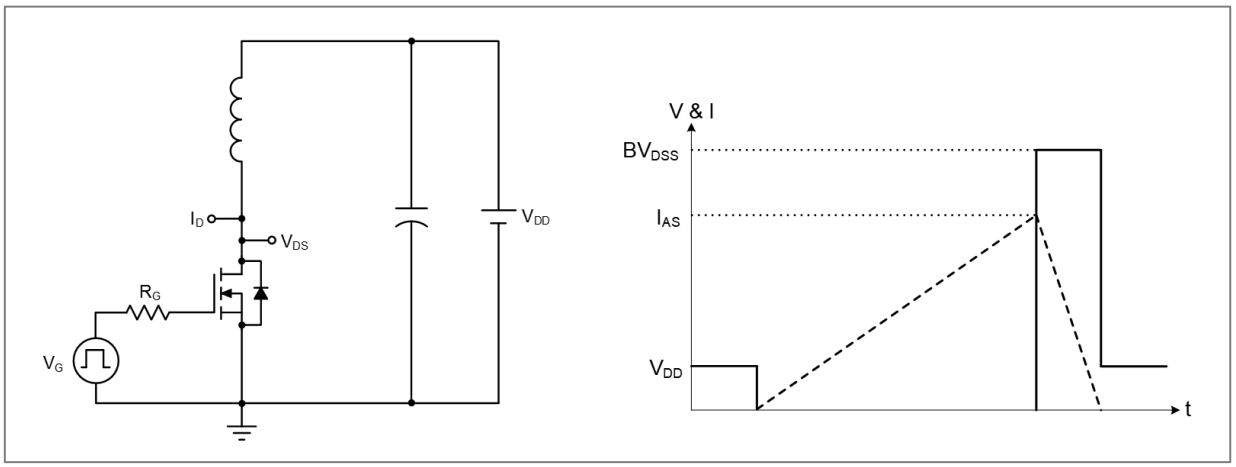
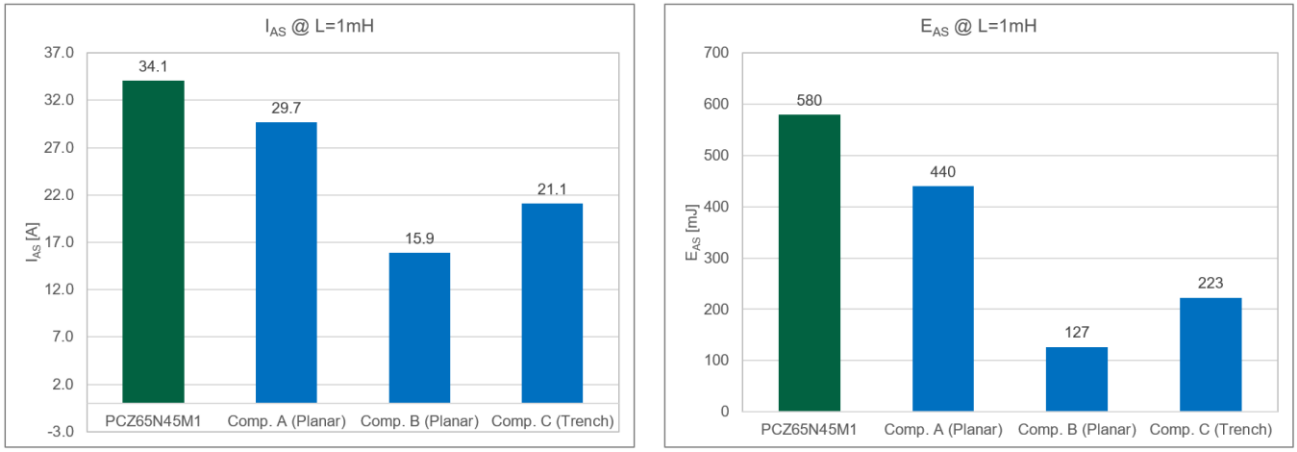


Figure 16. Unclamped Inductive Switching Test Circuit and Waveforms.

Typically, MOSFETs are employed in high-speed switching applications, therefore, electromagnetic force can be generated during turn-off transient by the abrupt changes of drain current from inductive loads. These forces may push the MOSFET into avalanche breakdown, potentially damaging it. Fig. 17 shows avalanche current (I_{AS}) and energy (E_{AS}) measurements of the 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) compared to competitor under same condition. The avalanche current (I_{AS}) and the avalanche energy (E_{AS}) of 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) are respectively 1.15 to 2.14 times higher and 1.32 to 4.58 times higher than those of both planar and trench SiC competitors. Fig. 18 shows drain current (I_D) and drain-source voltage (V_{DS}) waveforms during single pulse UIS test after failure under V_{DD}=70V, V_{GS}=-3/+18V, R_G=25Ω, L=1mH. The peak avalanche current (I_{AS}) gradually increases as the pulse width is increased until the device reaches its failure point. Upon failure, the voltage drops sharply, and the current begins to increase again linearly, as dictated solely by the inductor. After avalanche failure, the peak drain current of 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) and competitors are as follows. Power Master Semiconductor's 650V *e*SiC MOSFET offers 100% tested avalanche capability.

- PCZ65N45M1 : 37.9A
- Competitor A : 30.2A
- Competitor B : 17.4A
- Competitor V : 22.1A



(a) Single Pulsed Avalanche Current (b) Single Pulsed Avalanche Energy

Figure 17. Avalanche Capability under V_{DD}=70V, V_{GS}=-3/+18V, R_G=25Ω, L=1mH

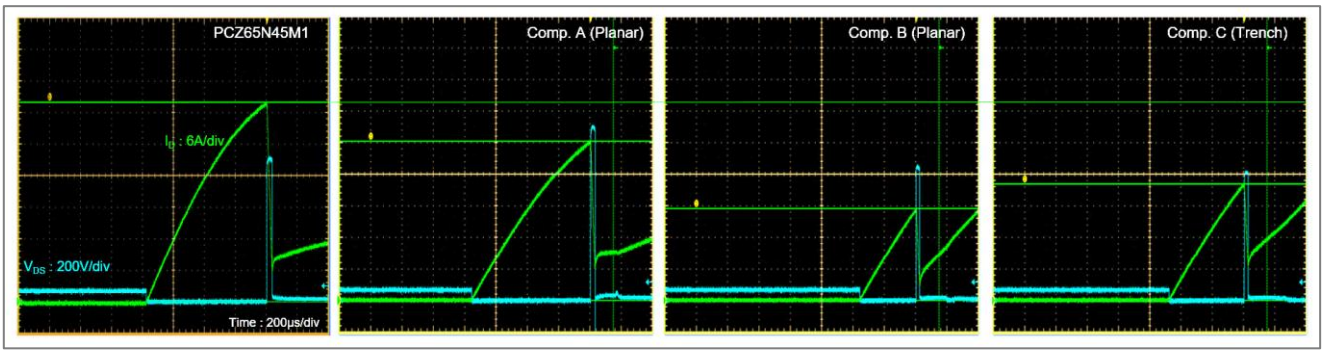


Figure 18. Waveforms during Single Pulse Avalanche (EAS) Test after Failure under V_{DD}=70V, V_{GS}=-3/+18V, R_G=25Ω, L=1mH

3.1.4. System efficiency comparison in 3kW CCM Totem-pole PFC

The system efficiency and switching noise of the 650V *e*SiC MOSFET M1 (PCZ65N45M1) are compared with those of competitor's 650V trench and planar SiC MOSFETs (DUTs), which is described in table 1, in a 3kW Continuous Conduction Mode (CCM) Totem-pole PFC. Fig. 19 illustrates the block diagram of the 3kW CCM totem-pole PFC using SiC MOSFETs. Two SiC MOSFETs (Q1 and Q2) in fast leg operate at a switching frequency of 65kHz, while another two MOSFETs (Q3 and Q4), which are 650V/28mΩ SJ MOSFET (PMW60N028E7) in slow leg operate at line frequency (50/60Hz).

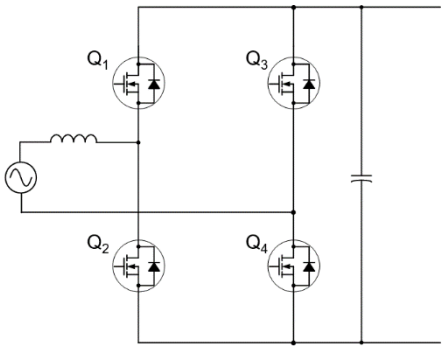


Figure 19. 3kW CCM Totem-Pole PFC Block Diagram

The measured efficiency is shown in Fig 20. The 650V *e*SiC MOSFET M1 (PCZ65N45M1) exhibits similar efficiency to the trench SiC competitor at half load and the highest efficiency, compared to competitor's planar and trench SiC MOSFETs at full load condition. The primary reason for higher efficiency is the reduced switch-off losses and output capacitive loss due to lower gate charger (Q_G) and dynamic C_{OSS} loss (E_{DYN}) of the 650V *e*SiC MOSFET M1. This MOSFET combines faster and more rugged avalanche performance, aimed at achieving improved reliability and efficiency in various applications. Fig. 21 shows the operating switching waveforms of V_{DS} and V_{GS} of both high side and low side MOSFETs during the low side MOSFET turn-off transient in a 3kW CCM Totem-Pole PFC under full load condition. As shown in Fig.21, the peak drain-source voltage (V_{DS}) and gate oscillation of 650V *e*SiC MOSFET M1 (PCZ65N45M1) are lower than those of competitor's planar and trench SiC MOSFETs. A unique advantage of the 650V *e*SiC MOSET is the lower voltage overshoot despite lower turn-off switching loss due to higher dv/dt compared to competitor's planar and trench SiC MOSFET. This unique switching characteristics of 650V *e*SiC MOSET can effectively reduce unwanted false turn-on and gate oxide damage failure during abnormal conditions.

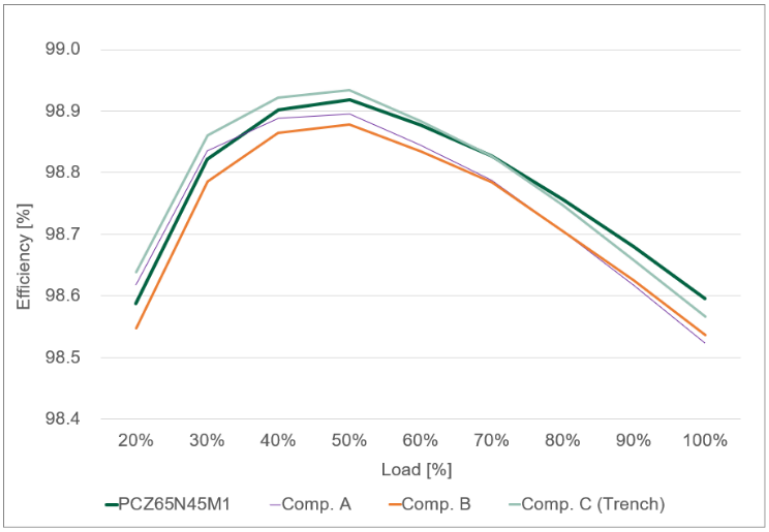
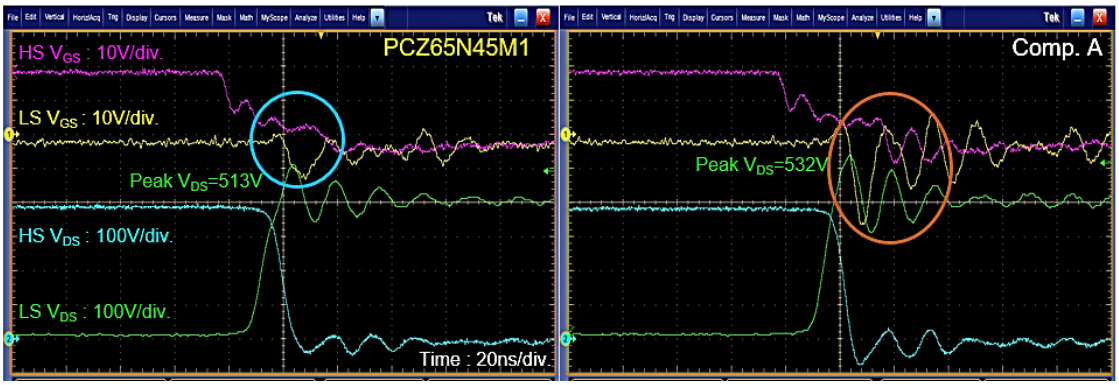
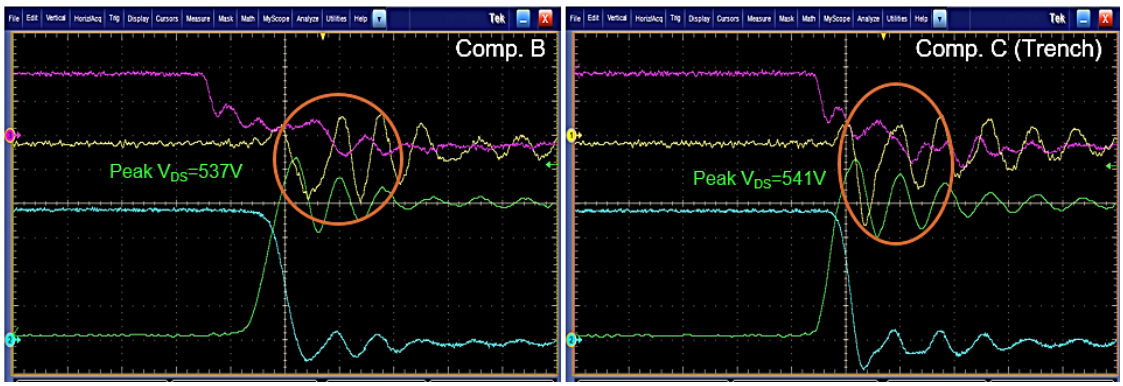


Figure 20. Measured Efficiency at 3kW CCM Totem-Pole



(a) PCZ65N45M1 (b) Comp. A (Planar)



(c) Comp. B (Planar) (d) Comp. C (Trench)

Figure 21. Measured Switching Waveforms during Low Side MOSFET Turn-Off Transient at 3kW CCM Totem-Pole PFC under V_{IN}=220V_{ac}, V_{GS}=-2.5/+18V, R_{ON}=22Ω / R_{OFF}=4.7Ω.

4. Conclusion

The latest 650V *e*SiC M1 MOSFET technology provides significantly low switching losses, minimized voltage spikes, low dynamic C_{OSS} loss and high UIS capability, even when compared with trench SiC MOSFETs. The 650V *e*SiC M1 technology is designed to achieve high efficiency and reliability by minimizing switching losses, dynamic C_{OSS}, as well as improving avalanche ruggedness in both hard and soft switching topologies.

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6. 650 eSiC MOSFET Product Portfolio & Nomenclature

6.1. 650V eSiC MOSFET Product Portfolio

Table 2. 650V eSiC MOSFET Product Portfolio

Solar | Server / Telecom | UPS | ESS PCS | EV(OBC) | EV Charger

Package / $R_{DS(ON)\_typ}$	Bare Die	TOLL	D2PAK-7L	TO-247-3L	TO-247-4L
					
15mΩ	PCO65N15M1	PCT65N15M1	PCBF65N15M1	PCW65N15M1	PCZ65N15M1
22mΩ	PCO65N22M1	PCT65N22M1			
27mΩ	**PCO65N27M1**	**PCT65N27M1**	PCBF65N27M1	**PCW65N27M1**	**PCZ65N27M1**
39mΩ	PCO65N39M1	PCT65N39M1			
45mΩ	**PCO65N45M1**	**PCT65N45M1**	PCBF65N45M1	**PCW65N45M1**	**PCZ65N45M1**

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6.2. Nomenclature

Device part number contains a lot of information such as technology, package, voltage rating and generation, etc. Figure 22 shows Power Master Semiconductor's eSiC MOSFET nomenclature

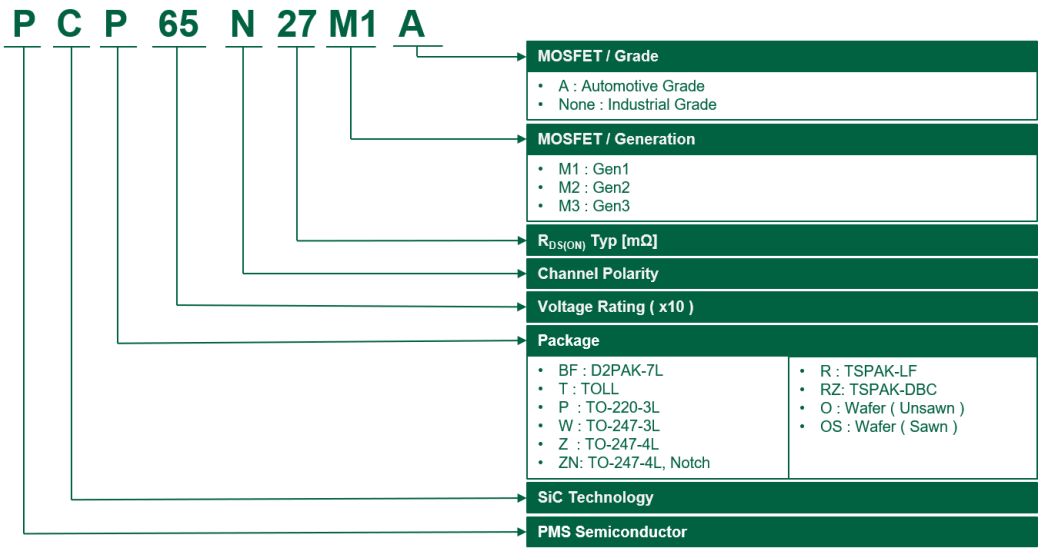

Figure 22. eSiC MOSFET nomenclature scheme

7. Document Revision History

Major changes since the last version

Date	Description of change
03-Sept-2024	First Release

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